CLAIMS:

1. A semiconductor processing method of forming a plurality of conductive lines comprising the following steps:

providing a substrate;

providing a first conductive material layer over the substrate;

providing a first insulating material layer over the first conductive layer;

etching through the first insulating layer and the first conductive layer to the substrate to both form a plurality of first conductive lines from the first conductive layer and provide a plurality of grooves between the first lines, the first lines being capped by first insulating layer material, the first lines having respective sidewalls;

electrically insulating the first line sidewalls; and

after insulating the sidewalls, providing the grooves with a second conductive material to form a plurality of second lines within the grooves which alternate with the first lines.

2. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

3. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the first and second conductive materials are the same material.

4. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the first and second conductive materials are different materials.

5. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the first conductive material comprises undoped polysilicon and the second conductive material comprises metal.

6. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the first conductive material comprises doped polysilicon and the second conductive material comprises metal.

7. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the grooves have respective open widths, and the step of electrically insulating the first line sidewalls comprises:

depositing a second insulating material layer over the etched first insulating and first conductive layers and the first line sidewalls to a thickness which is less than one-half the respective groove open widths to less than completely fill the grooves; and

anisotropically etching the second insulating material layer to define insulating sidewall spacers over the first line sidewalls.

8. The semiconductor processing method of forming a plurality of conductive lines of claim 1 wherein the step of providing the grooves with a second conductive material comprises:

depositing a second conductive material layer to a thickness effective to fill the grooves; and

without photomasking, planarize etching the second conductive material layer to form the plurality of second lines within the grooves.

9. The semiconductor processing method of forming a plurality of conductive lines of claim 1 further comprising forming a contact opening into the substrate prior to providing the grooves with the second conductive material.

10. The semiconductor processing method of forming a plurality of conductive lines of claim 1 further comprising forming a plurality of series of the first and second conductive lines at multiple elevations relative to the substrate.

11. A semiconductor processing method of forming a plurality of conductive lines comprising the following steps:

providing a substrate;

providing a first conductive material layer over the substrate;

providing a first insulating material layer over the first conductive layer;

etching through the first insulating layer and the first conductive layer to the substrate to both form a plurality of first conductive lines from the first conductive layer and provide a plurality of grooves between the first lines, the first lines being capped by first insulating layer material, the first lines having respective sidewalls, the grooves having respective open widths;

depositing a second insulating material layer over the etched first insulating and first conductive layers and the first line sidewalls to a thickness which is less than one-half the respective groove open widths to less than completely fill the grooves;

anisotropically etching the second insulating material layer to define insulating sidewall spacers over the first line sidewalls;

after providing the insulating sidewall spacers, depositing a second conductive material layer to a thickness effective to fill the remaining grooves; and

without photomasking, planarize etching the second conductive material layer to form a plurality of second lines within the grooves which alternate with the first lines.

12. The semiconductor processing method of forming a plurality of conductive lines of claim 11 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

13. The semiconductor processing method of forming a plurality of conductive lines of claim 11 wherein the first and second conductive materials are the same material.

14. The semiconductor processing method of forming a plurality of conductive lines of claim 11 wherein the first and second conductive materials are different materials.

15. The semiconductor processing method of forming a plurality of conductive lines of claim 11 wherein the first conductive material comprises undoped polysilicon and the second conductive material comprises metal.

16. The semiconductor processing method of forming a plurality of conductive lines of claim 11 wherein the first conductive material comprises doped polysilicon and the second conductive material comprises metal.

17. The semiconductor processing method of forming a plurality of conductive lines of claim 11 wherein the first and second insulating materials predominately comprise SiO_2.

18. The semiconductor processing method of forming a plurality of conductive lines of claim 11 further comprising forming a contact opening into the substrate prior to depositing the second conductive material.

19. The semiconductor processing method of forming a plurality of conductive lines of claim 11 further comprising forming a plurality of series of the first and second conductive lines at multiple elevations relative to the substrate.

20. A semiconductor processing method of forming a plurality of conductive lines comprising the following steps:

providing a substrate;

providing a first conductive material layer over the substrate;

etching through the first conductive layer to the substrate to both form a plurality of first conductive lines from the first conductive layer and provide a plurality of grooves between the first lines, the first lines having respective sidewalls;

electrically insulating the first line sidewalls; and

after insulating the sidewalls, providing the grooves with a second conductive material to form a plurality of second lines within the grooves which alternate with the first lines.

21. The semiconductor processing method of forming a plurality of conductive lines of claim 20 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

22. The semiconductor processing method of forming a plurality of conductive lines of claim 20 wherein the first and second conductive materials are the same material.

23. The semiconductor processing method of forming a plurality of conductive lines of claim 20 wherein the first and second conductive materials are different materials.

24. The semiconductor processing method of forming a plurality of conductive lines of claim 20 wherein the grooves have respective open widths, and the step of electrically insulating the first line sidewalls comprises:

depositing a second insulating material layer over the etched first conductive layers and the first line sidewalls to a thickness which is less than one-half the respective groove open widths to less than completely fill the grooves; and

anisotropically etching the second insulating material layer to define insulating sidewall spacers over the first line sidewalls.

25. The semiconductor processing method of forming a plurality of conductive lines of claim 20 wherein the step of providing the grooves with a second conductive material comprises:

depositing a second conductive material layer to a thickness effective to fill the grooves; and

without photomasking, planarize etching the second conductive material layer to form the plurality of second lines within the grooves.

26. The semiconductor processing method of forming a plurality of conductive lines of claim 20 wherein the grooves have respective open widths, and the step of electrically insulating the first line sidewalls comprises:

depositing a second insulating material layer over the etched first conductive layers and the first line sidewalls to a thickness which is less than one-half the respective groove open widths to less than completely fill the grooves; and

anisotropically etching the second insulating material layer to define insulating sidewall spacers over the first line sidewalls; and

the step of providing the grooves with a second conductive material comprises:

depositing a second conductive material layer to a thickness effective to fill the grooves; and

without photomasking, planarize etching the second conductive material layer to form the plurality of second lines within the grooves.

27. Integrated circuitry comprising:

a substrate; and

a series of alternating first and second conductive lines provided relative to the substrate, the first and second lines being spaced and positioned laterally adjacent one another relative to the substrate, the first lines and the second lines being electrically isolated from one another laterally by intervening anisotropically etched insulating spacers formed laterally about only one of the first or second series of lines.

28. The integrated circuitry of claim 27 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

29. The integrated circuitry of claim 27 wherein the first and second conductive lines constitute the same materials.

30. The integrated circuitry of claim 27 wherein the first and second conductive lines constitute different materials.

31. The integrated circuitry of claim 27 wherein the first conductive lines predominately comprise undoped polysilicon and the second conductive lines predominately comprise metal.

32. The integrated circuitry of claim 27 wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

33. The integrated circuitry of claim 27 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

34. Integrated circuitry comprising:

a substrate; and

a series of alternating first and second conductive lines provided relative to the substrate, the first and second lines being spaced and positioned laterally adjacent one another relative to the substrate, the first lines and the second lines being electrically isolated from one another laterally by intervening strips of insulating material, the first lines having a substantially common lateral cross sectional shape and the second lines having a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

35. The integrated circuitry of claim 34 wherein the first and second conductive lines constitute the same materials.

36. The integrated circuitry of claim 34 wherein the first and second conductive lines constitute different materials.

37. The integrated circuitry of claim 34 wherein the first conductive lines predominately comprise undoped polysilicon and the second conductive lines predominately comprise metal.

38. The integrated circuitry of claim 34 wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

39. The integrated circuitry of claim 34 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.